REMARKS

The remainder of this Amendment is set forth under appropriate subheadings for the convenience of the Examiner.

1. Status of the Claims

Claims 1 through 20 are pending in the instant patent applications. Claims 1, and 10 are independent. Claims 19 and 20 are new, and depend from independent Claim 1. Support for new Claims 19-20 can be found at various portions of the Applicant's specification including, for example, at FIG. 4, and at page 5, line 25 through page 7, line 4, and at various other locations of the written description.

2. Rejection of Claims 1 and 10 under 35 U.S.C. § 102(e)

In the Action, the Office rejects Claims 1 and 10 under 35 U.S.C. § 102(e) in view of United States Patent Application Publication No. US 2002/0054005 A1 to Edwards *et al.* (hereinafter "Edwards"). Applicant respectfully traverses the rejection by stating the Edwards does not disclose or suggest all of the elements of independent Claim 1.

Claim 1 recites a data scanner for driving a liquid crystal display (LCD). The data scanner includes a data bus containing digital data, and a row buffer coupled to the data bus for receiving and distributing the digital data received from the data bus. The data scanner also includes a switch network coupled to the row buffer. The switch network converts digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD. Similarly, Claim 10 is a method for driving an LCD and include the step of converting digital data to analog data using column load capacitances on pairs of column lines of the LCD.

The present disclosure eliminates the need for specific switched capacitor digital-to-analog converters and their associated amplifiers. Instead, the present disclosure uses the column line capacitances 160 (FIG. 4) along lines 135 to convert a digital signal to an analog signal. Here, row buffer 110 distributes digital data arriving from bus 130 to switches 410 on a pulse that is received from clock 120. The switches 410 convert the data using capacitance 160

shown in FIG. 4. See Applicant's specification at page 5, line 25 through page 6, line 5, and at FIG. 4.

Edwards does not disclose or suggest a switch network that converts digital data received from the row buffer to analog data by using column load capacitances on pairs of column lines of the LCD. The Examiner relies upon FIG. 1. At page 2 of Edwards, the reference clearly shows that a liquid crystal display includes a row and a column of picture elements. The picture elements 12 including switching TFTs 16, which are connected to sets of conductors 18 and 19.

The picture elements are formed from display elements that are located on electrodes carried by opposing surfaces of first and second substrates. See Edwards at paragraph 21.

Drive signals for driving the picture elements are supplied from a peripheral drive circuit, and switching waveforms are applied by timing circuits. Edwards discloses at paragraphs 22-25, that charge sharing occurs between two halves of the column capacitance, or along a length of the column conductor electrode 19 as shown in FIG. 2. Edwards also teaches at page 1, paragraph 3, a charge of a capacitor element, which is divided into two sub capacitor elements is shared.

There is no disclosure in Edwards of converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD. Thus, Claims 1 and 10 are novel over Edwards, under 35 U.S.C. § 102(e).

3. Rejection of Claims 2-8 under 35 U.S.C. § 103(a)

In the Action, Claims 2 through 8, and 11 through 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Edwards in view of United States Published Patent Application No. 2002/0135557A1 to Janssen et al. (hereinafter "Janssen"). The Action states that Janssen is cited to show that, connecting a switching device to adjacent column lines 80A and 80B of an LCD wherein a first column of the pair is coupled to alternating pixels of the first column line, is "old."

Janssen discloses a multiplexer at FIG. 3 that is connected to column lines 80A and 80B of a liquid crystal display. Janssen also teaches at paragraphs 2 and 7, that each column is split into two column lines, and by this "splitting of the column lines" the capacitance of each line is a fraction of that required by a single column, and reduces the capacitance load on the columns.

Janssen does not remedy the deficiencies of Edwards. Neither Edwards nor Janssen, together or in combination, disclose or suggest converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD, as in Applicant's Claims 1 and 10. Therefore, independent Claims 1 and 10 meet the requirements of 35 U.S.C. § 103(a), in view of Edwards and Janssen, taken separately or in combination. Accordingly, Claims 2 through 8 are patentable, as these claims depend on Claim 1. Claims 11 through 17 are also patentable, as they depend from independent Claim 10. Reconsideration and withdrawal of the rejection of Claims 2-8, and 11-17 under 35 U.S.C. § 103(a) are requested.

4. Rejection of Claims 9 and 18 under 35 U.S.C. § 103(a)

In the Action, Claim 9 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Edwards in view of United States Patent No. 5,619,225 to Hashimoto *et al.* (hereinafter "Hashimoto"). Specifically, the Office contends that Hashimoto discloses a delta layout pixel arrangement in FIGS. 4 and 5.

Hashimoto discloses at Column 2, line 64 through Column 3, line 6, that the unit of the pixel of the display element section 410 is formed of a switching transistor 411, and a pixel holding capacitance 412. The other terminal of the pixel holding capacitance 412 is connected to an electrode voltage V_{LC}. Color signals are sent from a processing circuit to a sampling circuit 430. In a control circuit 460, the necessary pulses are formed and are supplied to the vertical scanning circuit 420, the horizontal scanning circuit 440, and the signal processing circuit 450. Hashimoto further discloses that the signal processing circuit is connected to an amplifier 480 in FIG. 20.

Like Edwards, Hashimoto does not disclose or suggest converting digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD as claimed in Claim 1. Claim 9 and 18 depend from independent Claims 1 and 10, respectively. Therefore, neither Edwards not Hashimoto, taken separately or in combination, disclose or suggest Applicant's claimed invention as set forth in dependent Claims 9 and 18. Reconsideration and withdrawal of the rejection of Claims 9 and 18 under 35 U.S.C. § 103(a) are respectfully requested.

5. New Claims 19 and 20

Applicant has added new dependent Claims 19 and 20 to the instant application. New Claim 19 depends from Claim 1 and recites that the switch network converts digital data received from the row buffer to analog data using column load capacitances on pairs of column lines of the LCD. The pairs include at least a first column line and a second column line wherein the switch network is connected to each of the first and the second column lines. New Claim 20 depends from Claim 19 and further recites that the first and the second column line are separate and spaced from one another. Support for new Claims 19-20 can be found at various portions of the Applicant's specification including, for example, at FIG. 4, and at page 5, line 25 through page 7, line 4, and at various other locations of the written description. Allowance of Claims 19 and 20 are respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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